IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 1, January 2016

A Novel Fine Trench MOSFET with High Voltage Isolation for Smart Power System

Kumar Arvind[1], Vijay Sharma[2], Dr. U.B.S. Chandrawat[3]

Dept of Electronics and Communication Engineering, Swami Vivekanand College of Engineering, Indore, India[1, 2, 3]

Abstract: This paper present a Fine Trench power MOSFET with having low On-state resistance for high voltage applications. Day to day advancement in silicon power MOSFET highly improved performance has been achieved with vertical structure of Trench gate. Recent research in metal oxide semiconductor field effect transistor enables very compact high efficient system design with enhanced power gain for high voltage isolated devices. The proposed novel fine Trench MOSFET is designed with n- epitaxial layer between two Trench gate. The deep Trench high voltage isolated design is simulated with SILVACO TCAD simulator.

Keywords: Fine Trench MOSFET, SILVACO TCAD, Deep Trench Architecture, On-state Resistance.

1. INTRODUCTION

In modern technologies, introduction of new electronic devices have required significant power levels. Devices like consumer and automatic applications based has the integral requirement of high voltages range of 20V to 100V. To achieve power level for various devices several power MOSFET's are available. This paper proposed a novel fine Trench MOSFET with low on-state resistance. Trench power MOSFET is well known for its low on-state resistance and improved breakdown voltages. In novel fine Trench MOSFET at high voltage on-state resistance and energy efficient high side capability implemented with minimum epitaxial thickness. This power MOSFET doesn't have p-base region n+ substrate and n-well region. Low on-state resistance is occurred by Trench gate sidewall layer accumulation. Novel fine Trench is much effective as per concern of its design, complexity, heat removal ability with suitable power ranges. In this paper we proposed a Novel fine Trench power MOSFET with its effective on-state resistance and improved breakdown voltage that is suitable for significant power level.

Novel fine Trench MOSFET is a power MOSFET in which Trench gate is the mainstream classified under low voltage MOSFET. The proposed fine Trench is designed as figure 1. The structure presented with deep Trench gate in which Trench gate doesn't reach till the n+ substrate. Doping concentration of n-drift layer is kept intermediate and placed between the substrate and fine Trench bottom. The n-epitaxial is depleted as the potential of Trench gate poly. Generally fine Trench MOSFET has off-state characteristics without p-base region. According to previous research less than 0.4 μm separation of Trench to Trench and n-epitaxial impurity concentration of 1×10^{-15} cm^{-3} require for off-state operation. Positive voltage at Trench gate induces low resistance in Trench sidewalls. Drain current flows into accumulation layer from n-drift region. Advance Trench power MOSFET's popularly used in many switching applications. To enhance efficiency and minimization of losses occurred in switching is achieved by improvement of on-state resistance.

A higher doping concentration in drift region of fine Trench power MOSFET enables the reduction of

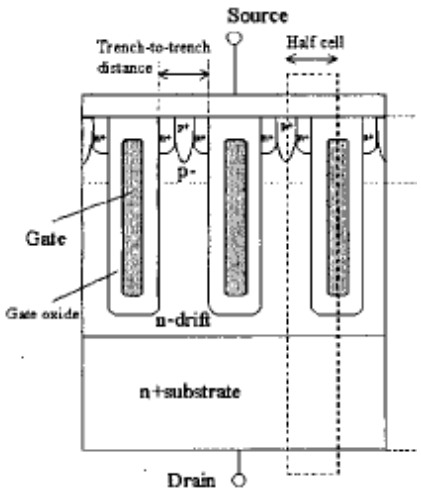

Figure 1: Fine Trench MOSFET Structure

resistance occurrence for the required breakdown voltages. By removal of junction field effect region low on-state resistance is achieved. Resistance in drift region is the combination of two components as n-type drift region and substrate. The specific on- state resistance can be calculated as-

$$R_{DS(ON)} = (BV/ (\varepsilon_S \times \mu_N \times E_{CU}^2)) \times (W_N + W_P)/2$$

Where

BV = Break down voltage
ε_S = Dielectric constant
μ_N = Electron mobility
E_{CU} = Critical electric field
W_N and W_P = Width in N type and P type drift region

Power dissipation in fine Trench MOSFET is the allowable power limit. The power dissipation parameters are basically dependent on case temperature and ambient temperature. Parameters can be calculated as-

$$P_D (T_C) = (T_J - T_C)/ R_{\theta JC}$$

$$P_D (T_A) = (T_J - T_A)/ R_{\theta JC}$$

DOI 10.17148/IJIREEICE.2016.4118

IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 1, January 2016

Where
T_J = Junction Temperature
T_C = Case Temperature
T_A = Ambient Temperature
$R_{\theta JC}$ = Junction-to-Case Thermal Resistance

2. DESIGN AND SIMULATION PARAMETERS

A simple 2D structure of fine Trench MOSFET is shown in figure 2.1. It has a fine deep Trench into N- substrate. Trench is made with oxide and filled with polysilicon to design Trench gate. The upper design have a thin oxide grown to form conventional metal oxide semiconductor gate to make it vertical channel structure and lower side have thick oxide serves as depletion of N- drift region. Structural layout design of Fine Trench is shown in figure 2.2. Device is simulated with Dev Edit SILVACO platform and composed of silicon, SiO_2 and polysilicon.

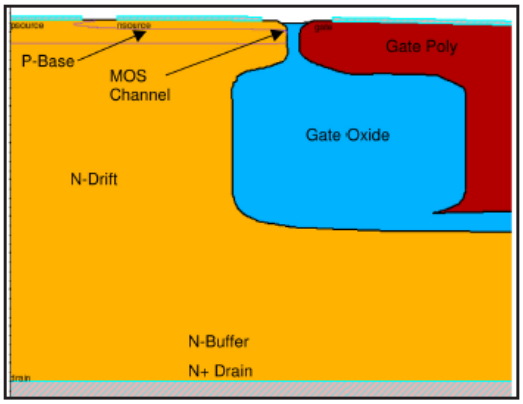

Fig. 2.1: Half Cell of Fine Trench Power MOSFET

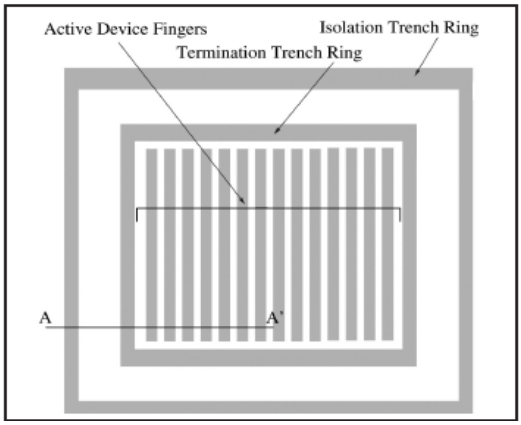

Fig. 2.2: Layout Design Structure

The termination trench gate structure considered in design is similar to the active trench except that the thick oxide layer extends the full depth of the trench gate. Doping concentration of drift region is kept as 1.5×10^{17} cm^{-3} and N-substrate concentration is 2.7×10^{17} cm^{-3}. The doping profile between drift region and substrate region is estimated out-diffusion of substrate layer.

3. SIMULATIONS AND DISCUSSION

The Fine trench MOSFET design is simulated with SILVACO TCAD. Figure 3.1 shows the output characteristics. The curve shows the functional relation of drain current Vs drain to source voltages. Through the output curve we observe at 12 V drain current slightly increasing. This is the voltage range which marked as breakdown voltage for this proposed design. Figure 3.2 shows the other parameters like gate voltage and drain to source voltage.

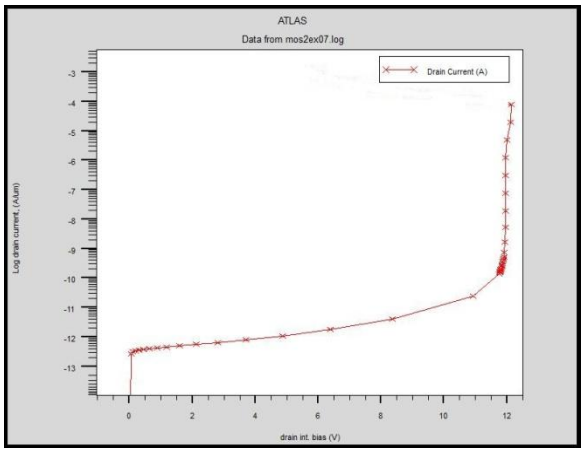

Fig. 3.1: Output Characteristics for Fine Trench MOSFET

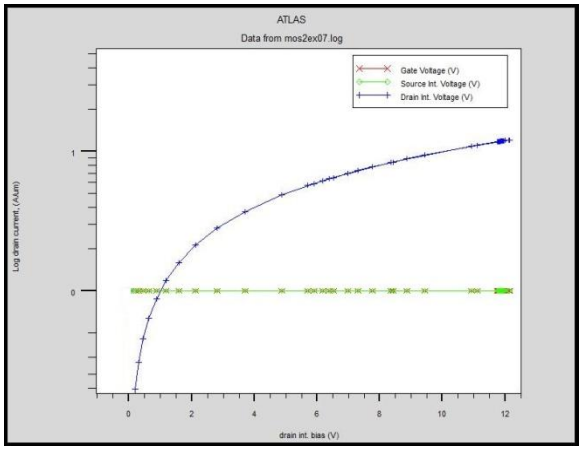

Fig. 3.2: Gate and Source Voltages

Output curve of Fine Trench shows slightly different aspects as to rise of drain to source voltages. The rising curve from 0.5V to 10.5V of drain current is limited by on-state resistance. After 12V the drain current curve is limited because of maximum power dissipation. The gate voltage and source voltage is kept ideally 0V here. Transfer characteristics are used to analyse the threshold voltage of device can be shown as the intercept point of maximum slope with gate voltage axis of Fine Trench. On-state resistance can be estimated for this model with the following parameters.

$$R_{DS(ON)} = \quad (BV/ (\varepsilon_S \times \mu_N \times E_{CU}^2)) \times (W_N + W_P)/2$$

Taking the appropriate value in the above we observed the on-state resistance for Novel fine trench design is 7 $m\Omega/cm^3$. Breakdown voltage is observed from the output characteristics curve is 12V. The drain current (I_D) observed in output curve is differ with various drain to source voltages not by gate to source voltages. All the smart power devices operate in linear region. To enhance

the drain current, drain to source voltage should applied to the gate.

4. CONCLUSION

In conclusion, we have successfully simulated the proposed model and analysed the experimental data of Novel Fine Trench MOSFET. The proposed fine Trench has marked as low on-state resistance by utilizing the accumulation effect. For this design breakdown voltage is observed as 12V. On-state resistance is reported as7 $m\Omega/cm^3$. The observed result shows that the specific on-state resistance depends on the concentration and width of Fine Trench gate pillar. Optimization of Fine Trench MOSFET has positive symbols in the utility of smart power technology.

REFERENCES

[1] Fully self aligned power Trench MOSFET utilizing 1um pitch and 0.2 um Trench width by Steven T. Peake IEEE 2002.
[2] An Ultra Dense Trench Gated Power MOSFET Technology using a self aligned Process by Jun Zeng, ISPSD 2002.
[3] B.J Baliga, Advance Power MOSFET Concepts, New York Springer Science, 2010.
[4] 30V New Fine Trench MOSFET with Ultra Low On- Resistance by Syotaro Ono,ISPSD 2003, Cambridge,UK
[5] R Vaid and N Padha Indian Journal Engineering and material Science, 13 2006.
[6] A. Moscatelli et al, ISPSD, 2000.
[7] Wilson, Peter H. "Automotive MOSFETs in Linear Applications: Thermal Instability," Application Note V1.0, May 2005.
[8] SILVACO TCAD Manual, Atlas, 2011
[9] C. Blake, and A. Arzumanyan, "Evaluating the reliability of power MOSFETs", Power Electronics Technology, 2005, pp. 40-44.
[10] A. Kwan and T. McDonald,"Improved SOA analysis for trench MOSFETs using the Spirito approach", 9th Annual Automotive Electronics Reliability Workshop,2004